- **Contain Six Flip-Flops With Single-Rail Outputs**

- **Applications Include:**
  - **Buffer/Storage Registers**
  - **Shift Registers**
  - **Pattern Generators**

- **Package Options Include Plastic Small-Outline (D) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**
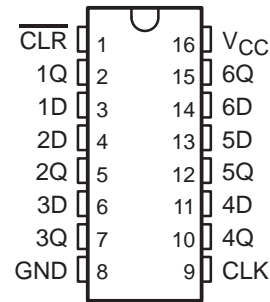
SN54HC174 . . . J OR W PACKAGE
SN74HC174 . . . D OR N PACKAGE
(TOP VIEW)

$\overline{CLR}$	1	16 V_{CC}
1Q	2	15 6Q
1D	3	14 6D
2D	4	13 5D
2Q	5	12 5Q
3D	6	11 4D
3Q	7	10 4Q
GND	8	9 CLK

SN54HC174 . . . FK PACKAGE
(TOP VIEW)

Top pins: 1Q, $\overline{CLR}$, NC, V_{CC}, 6Q (pins 3 2 1 20 19)

1D	4	18 6D
2D	5	17 5D
NC	6	16 NC
2Q	7	15 5Q
3D	8	14 4D

Bottom pins: 3Q, GND, NC, CLK, 4Q (pins 9 10 11 12 13)

NC – No internal connection

description

These monolithic positive-edge-triggered D-type flip-flops have a direct clear ($\overline{CLR}$) input.
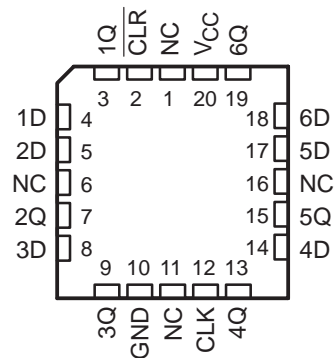
Information at the data (D) inputs meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going edge of CLK. When CLK is at either the high or low level, the D input has no effect at the output.

The SN54HC174 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC174 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
$\overline{CLR}$	CLK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

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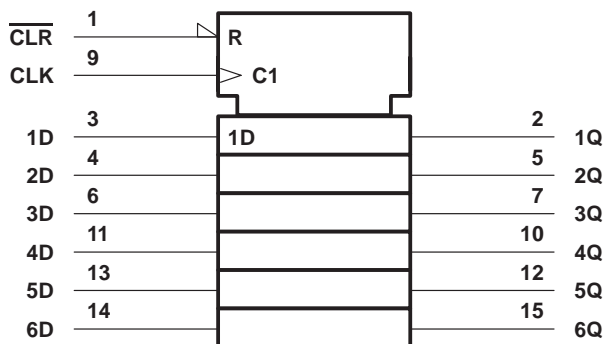
logic symbol[†]

[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, and W packages.

logic diagram (positive logic)

To Five Other Channels
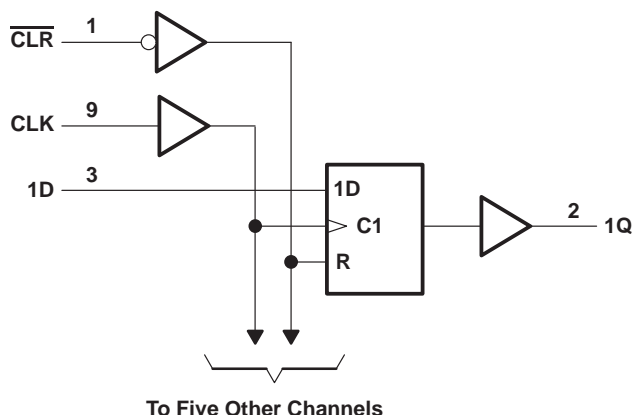
Pin numbers shown are for the D, J, N, and W packages.

absolute maximum ratings over operating free-air temperature range[‡]

Supply voltage range, V_{CC} .... −0.5 V to 7 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) (see Note 1) .... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) (see Note 1) .... ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) .... ±25 mA
Continuous current through V_{CC} or GND .... ±50 mA
Package thermal impedance, θ_{JA} (see Note 2): D package .... 113°C/W
                                                    N package .... 78°C/W
Storage temperature range, T_{stg} .... −65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and
   functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not
   implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
         2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace
             length of zero.

recommended operating conditions

			SN54HC174			SN74HC174			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.5	0		0.5	V
		V_{CC} = 4.5 V	0		1.35	0		1.35	
		V_{CC} = 6 V	0		1.8	0		1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC174		SN74HC174		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH}$ or V_{IL}	I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I_{OH} = −4 mA	4.5 V	3.98	4.3		3.7		3.84		
		I_{OH} = −5.2 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}	$V_I = V_{IH}$ or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	$V_I = V_{CC}$ or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	$V_I = V_{CC}$ or 0, I_O = 0		6 V			8		160		80	μA
C_i			2 V to 6 V		3	10		10		10	pF

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SN54HC174, SN74HC174
HEX D-TYPE FLIP-FLOPS
WITH CLEAR

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V_{CC}	$T_A = 25°C$ MIN	$T_A = 25°C$ MAX	SN54HC174 MIN	SN54HC174 MAX	SN74HC174 MIN	SN74HC174 MAX	UNIT
f_{clock}	Clock frequency	2 V	0	6	0	4.2	0	5	MHz
		4.5 V	0	31	0	21	0	25	
		6 V	0	36	0	25	0	29	
t_w	Pulse duration	$\overline{CLR}$ low 2 V	80		120		100		ns
		$\overline{CLR}$ low 4.5 V	16		24		20		
		$\overline{CLR}$ low 6 V	14		20		17		
		CLK high or low 2 V	80		120		100		
		CLK high or low 4.5 V	16		24		20		
		CLK high or low 6 V	14		20		17		
t_{su}	Setup time before CLK↑	Data 2 V	100		150		125		ns
		Data 4.5 V	20		30		25		
		Data 6 V	17		25		21		
		$\overline{CLR}$ inactive 2 V	100		150		125		
		$\overline{CLR}$ inactive 4.5 V	20		30		25		
		$\overline{CLR}$ inactive 6 V	17		25		21		
t_h	Hold time, data after CLK↑	2 V	0		0		0		ns
		4.5 V	0		0		0		
		6 V	0		0		0		

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)
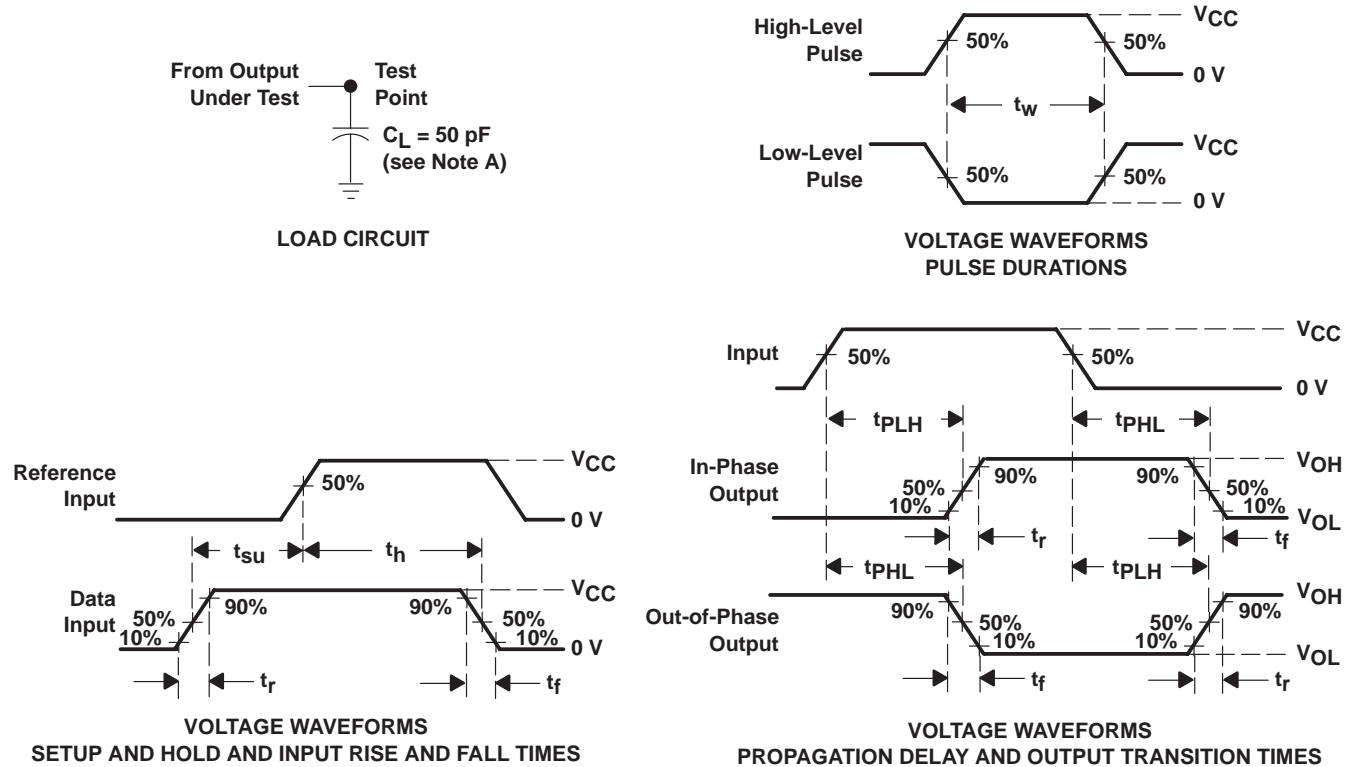
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25°C$ MIN	$T_A = 25°C$ TYP	$T_A = 25°C$ MAX	SN54HC174 MIN	SN54HC174 MAX	SN74HC174 MIN	SN74HC174 MAX	UNIT
f_{max}			2 V	6	9		4.2		5		MHz
			4.5 V	31	44		21		25		
			6 V	36	50		25		29		
t_{pd}	$\overline{CLR}$	Any	2 V		58	160		240		200	ns
			4.5 V		17	32		48		40	
			6 V		14	27		41		34	
	CLK	Any	2 V		58	160		240		200	
			4.5 V		17	32		48		40	
			6 V		14	27		41		34	
t_t		Any	2 V		38	75		110		90	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

operating characteristics, $T_A = 25°C$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance per flip-flop	No load	27	pF

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PARAMETER MEASUREMENT INFORMATION

LOAD CIRCUIT

From Output Under Test — Test Point

$C_L = 50\ pF$
(see Note A)

**VOLTAGE WAVEFORMS
PULSE DURATIONS**

High-Level Pulse — 50% — 50% — V_{CC} / 0 V — t_w

Low-Level Pulse — 50% — 50% — V_{CC} / 0 V

**VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES**

Reference Input — 50% — V_{CC} / 0 V

t_{su} t_h

Data Input — 50% 10% — 90% — 90% — 50% 10% — V_{CC} / 0 V

t_r t_f

**VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES**

Input — 50% — 50% — V_{CC} / 0 V

t_{PLH} t_{PHL}

In-Phase Output — 50% 10% — 90% — 90% — 50% 10% — V_{OH} / V_{OL}

t_r t_f

t_{PHL} t_{PLH}

Out-of-Phase Output — 90% — 50% 10% — 50% 10% — 90% — V_{OH} / V_{OL}

t_f t_r

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

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